the wall that includes a processing circuit electrically connected to the sensitive element on the first chip.

Flach et al., European Patent No. 0773443, is directed to a micromechanical accelerometer formed of two semiconductor wafers. The accelerometer operates on the basis of a variable capacitance between fixed electrodes 12', 12'' formed on a lower silicon wafer, and a movable electrode earthed by wafer bonding and pivoted on an axis below a second wafer, a silicon-on-insulator wafer. Acceleration in the vertical direction rocks the movable electrode so that capacitances between it and fixed electrodes on the lower wafer increase and decrease. A microelectronic processor is implemented on the lower wafer. Nowhere does Flach et al. teach or suggest the second wafer having a processing circuit that is in electrical contact with the accelerometer formed on the first wafer. Also, Flach et al. does not disclose or suggest hermetically sealing the accelerometer on the lower wafer. Hence, because the signal output by the accelerometer is already available on the lower chip, no electrical connection is provided between the two chips disclosed in Flach et al.

Otani et al., U.S. Patent No. 5,864,063, is directed to an electrostatic capacitor-type acceleration sensor that includes a mobile mass 14 enclosed in a hollow structure defined by a substrate 4, an auxiliary support 19, and a protection substrate 3 (see Otani et al., col. 4, lns. 1-3, and col. 6, lns. 46-47). The integrated circuit 6 is then bonded on top of the substrate 3 (see col. 3, lns. 16-17) by means of an adhesive layer 9 (see col. 3, lns. 29-30) or by the electrical connections with the sensor unit (see col. 5, lns. 35-48). Therefore, the integrated circuit 6 does not take part in forming the hollow structure. In contrast, the disclosed embodiments of the present invention include a second chip wherein processor circuitry is formed, the second chip defining a top wall of and directly delimiting the hollow structure formed in the first chip. The second chip is affixed to the wall, which laterally defines the hollow structure.

Ueda et al., U.S. Patent No. 5,650,567 is directed to an acceleration sensor with opposed amplifier and detection sections that, although disclosing the use of metal in forming a chamber, does not teach or suggest forming a sensor on a first chip that is surrounded by a wall and enclosed in a chamber created by the combination of the wall and a second chip attached to the wall, and an electrical connection between the second chip and first chip to process signals generated by the sensor on the first chip.

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Parsons, U.S. Patent No. 5,719,334, discloses a hermetically-protected sensor assembly that is filled with either a gel that is water-resistant or waterproofing silicon. However, Parsons does not teach or suggest the combination of first and second chips connected by a wall to form a hermetically-sealed chamber in which a sensor element is formed on the first chip and electrically connected to a processor on the second chip.

Turning next to the claims, claim 1 is directed to a sensor having a movable microstructure that comprises a sensitive element formed in a first chip of semiconductor material for producing an electrical signal dependent on a movement of at least one movable microstructure relative to a surface of the first chip. Claim 1 further recites the sensitive element being enclosed in a hollow hermetic structure, and a processing circuit for processing the electrical signal formed in a second chip of semiconductor material and in electrical connection with the electrical signal produced by the sensitive element formed in the first chip. Nowhere does Flach et al. or any combination of Otani et al. with Ueda et al. and Parsons teach, suggest, or disclose the formation of a sensitive element in a first chip that is enclosed in a hollow hermetic structure enclosed by a second chip that includes a processing circuit for processing an electrical signal generated from the first chip and connected electrically to the processing circuit on the second chip.

Claim 1 further recites the hollow hermetic structure including a metal wall disposed on a surface of the first chip around the sensitive element, the second chip being affixed to the wall. As discussed above, Otani et al. discloses an integrated circuit 6 that is bonded on top of a substrate 3, which is not part of the hollow structure defined by the substrate 4, the auxiliary support 19, and a protection substrate 3. In view of the foregoing, Applicants respectfully submit that claim 1 is clearly allowable over the references cited and applied by the Examiner.

Dependent claims 2-7 all depend from independent claim 1 and are similarly allowable. Moreover, dependent claims 3-5 recite at least one first, third, and fifth conductive pads formed on a surface of the first chip and at least one second, fourth, and sixth pads formed on the second chip for receiving electrical signals. Nowhere does Flach et al. or any combination of Otani et al. with Ueda et al. and Parsons teach or suggest such a connection in combination

with the elements of claim 1. Applicants respectfully submit that these dependent claims are therefore allowable for these reasons, as well as for the reasons why claim 1 is allowable.

Claim 12 is directed to a sensor comprising a first chip of semiconductor material, a sensor element having a movable structure, the sensor element being supported by the first chip and being structured to generate a first signal in response to movement relative to the first chip; a second chip of semiconductor material configured to receive the first signal; and a wall formed on the first chip surrounding the sensor element and connecting the first chip to the second chip to define a hermetically-sealed chamber enclosing the sensor element. As discussed above with respect to claim 1, Flach et al. does not teach or suggest a sensor element formed on a first chip to generate a first signal and surrounded by a wall formed on the first chip and connected to a second chip of semiconductor material that is configured to receive the first signal, with the second chip connected to the first chip through a surrounding wall that defines a hermetically-sealed chamber. Likewise, Otani et al. fails to disclose a second chip of semiconductor material configured to receive a first signal from the sensor element formed on the first chip of semiconductor material. In view of the foregoing, Applicants respectfully submit that claim 12 is allowable for these reasons as well as for the reasons why claim 1 is allowable.

Dependent claims 13-20 recite additional embodiments of the invention, including a processing circuit formed on the second chip of semiconductor material and electrically coupled to the sensor element to receive the first signal and to generate a second signal based on the first signal. Claim 16 recites a plurality of conductive pads connected between the first chip and the second chip and a low resistance to fusion in the first chip between the sensor elements and the pads. Nowhere do Flach et al. or any combination of Otani et al. with Parsons and Ueda et al. teach, suggest, or disclose the combination recited in these dependent claims in combination with claim 12. For these reasons, Applicants respectfully submit that dependent claims 13-20 are allowable as well as for the reasons why claim 12 is allowable.

In view of the foregoing, Applicants respectfully submit that all of the claims in this application are now clearly in condition for allowance. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited. In the event the Examiner finds minor informalities that can be addressed by telephone conference, the

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Examiner is urged to contact Applicants' undersigned representative at telephone (206) 622-4900.

Respectfully submitted,

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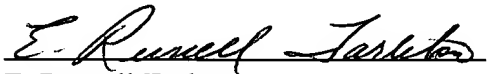

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